DECLARATION

I, the undersigned, Yoko OISHI, residing at 5-7-9-203, Minamiosawa, Hachioji Tokyo, JAPAN, do solemnly and sincerely declare that I well understand the Japanese language and the English language and that the attached English translation of a certified copy of Japanese Patent Application No. 2002-356291 is true, correct and faithful translation to the best of my knowledge and belief from the Japanese language into the English language.

Dated this 16th of December, 2008

Yoko OISHI

[Name of Document]	NATIONAL FORM PAPER
[Reference Number]	340P0004
[To]	Commissioner, Patent Office Hiroshi OGAWA
[Identification of the Application]	
[International Application Number]	PCT/JP03/12080
[Classification of Application]	Patent
[Inventor]	
[Address or Residence]	c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan
[Name]	Makoto UEKI
[Inventor]	
[Address or Residence]	c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan
[Name]	Masayuki HIROI
[Inventor]	
[Address or Residence]	c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan
[Name]	Nobuyuki IKARASHI
[Inventor]	
[Address or Residence]	c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo, Japan
[Name]	Yoshihiro HAYASHI
[Applicant]	
[Identification Number]	000004237
[Name]	NEC Corporation
[Agent]	
[Identification Number]	100090158
[Patent Attorney]	

[Name]	Masanori FUJIMAKI
[Indication of the Official Fee]	
[Prepayment Register Number]	009782
[Amount of Payment]	21,000 Yen
[List of Items Submitted]	
[General Power of Attorney Number]	9715181

[Name of the Document] SPECIFICATION

[Title of the Invention] METAL FOR WIRING, SEMICONDUCTOR DEVICE, AND MANUFACTURING METHOD THEREOF

[Claims]

[Claim 1] A metal for wiring that contains a multicrystal having Cu (copper) as a main component and an added element other than Cu, characterized in that

a concentration of the added element at a crystal grain boundary and a crystal grain boundary proximity of a crystal grain of the multicrystal is higher than that of the crystal grain interior.

[Claim 2] The metal for wiring according to claim 1, characterized in that the added element is an element of at least any one of Ti (titanium), Zr (zirconium), Hf (hafnium), Cr (chromium), Co (cobalt), Al (aluminum), Sn (tin), Ni (nickel), Mg (magnesium), and Ag (silver).

[Claim 3] The metal for wiring according to claim 1, characterized in that the crystal grain boundary and the crystal grain boundary proximity are formed of an intermetallic compound between Cu and an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[Claim 4] The metal for wiring according to claim 1, characterized in that the crystal grain boundary and the crystal grain boundary proximity contain an oxide of an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[Claim 5] The metal for wiring according to any one of claim 1 to claim 4, characterized in that a concentration of the added element of the crystal grain interior is at most 0.1 atomic %.

[Claim 6] A semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, characterized in that

the metal wiring comprises the metal for wiring according to any one of claim 1 to claim 5.

[Claim 7] A manufacturing method of a metal for wiring that contains a

multicrystal comprising Cu as a main component and an added element other than Cu, comprising:

a Cu multicrystal formation step that forms the multicrystal comprising Cu as a main component;

an added element layer formation step that forms a layer comprising the added element on the Cu multicrystal; and

an added element diffusion step that diffuses the added element into the Cu multicrystal.

[Claim 8]

The manufacturing method of a metal for wiring according to claim 7, characterized in that a heating step that heats the substrate having the formed Cu multicrystal, the added element layer formation step, and the added element diffusion step are performed simultaneously.

[Claim 9] The manufacturing method of a metal for wiring according to claim 7 or claim 8, characterized in that the added element is an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[Claim 10] A manufacturing method of a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, comprising:

a Cu multicrystal formation step that forms the multicrystal comprising Cu as a main component;

an added element layer formation step that forms a layer comprising the added element on the Cu multicrystal; and

an added element diffusion step that diffuses the added element into the Cu multicrystal.

[Claim 11] A manufacturing method of a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element,

comprising:

an insulative film formation step that forms an insulative film on the substrate;

a wiring recess formation step that forms a recess for wiring comprising at least either of a groove or a hole in the insulative film;

a Cu film formation step that forms Cu in a film to fill the wiring recess;

an excess Cu removal step that removes excess Cu other than Cu filled into the wiring recess by chemical mechanical polishing;

an added element layer formation step that forms a layer comprising the added element on the Cu formed in a film;

an added element diffusion step that diffuses the added element into Cu formed in a film; and

an excess added element removal step that removes an excess added element from the added element layer.

[Claim 12] A manufacturing method of a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, comprising:

an insulative film formation step that forms an insulative film on the substrate;

a wiring recess formation step that forms a recess for wiring comprising at least either of a groove or a hole in the insulative film;

a barrier metal film formation step that forms a barrier metal film, that prevents a diffusion of Cu, on the insulative film comprising the wiring recess;

a Cu film formation step that forms Cu in a film to fill onto the barrier metal film of the wiring recess;

an excess Cu removal step that removes excess Cu other than Cu filled into the wiring recess by chemical mechanical polishing;

a barrier metal film removal step that removes excess of an excess barrier metal film other than a barrier metal film filled into the wiring recess by chemical mechanical polishing;

an added element layer formation step that forms a layer comprising an added element on the Cu formed in a film;

an added element diffusion step that diffuses the added element into Cu formed in a film; and

an excess added element removal step that removes an excess added element from the added element layer.

[Claim 13] The manufacturing method of a semiconductor device according to any one of claim 11 or claim 12, characterized in that the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed prior to the excess Cu removal step.

[Claim 14] The manufacturing method of a semiconductor device according to any one of claim 11 or claim 12, characterized in that the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed after the excess Cu removal step.

[Claim 15] The manufacturing method of a semiconductor device according to any one of claim 10 to claim 14, characterized in that a heating step that heats the substrate, the added element layer formation step, and the added element diffusion step are performed simultaneously.

[Claim 16] The manufacturing method of a semiconductor device according to any one of claim 10 to claim 15, characterized in that the added element is an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a metal for wiring and a semiconductor device using the same, and in particular, relates to a structure of a copper metal for wiring having high reliability, a semiconductor device using the same, and a manufacturing method therefor.

[0002]

[Prior Art]

Conventionally, aluminum (Al) or Al alloy has been widely used as a wiring material of semiconductor devices. However, accompanying the progress of miniaturization and increased speeds of semiconductor devices, the transfer delay of wiring is being improved while being able to use copper (Cu) having lower resistivities as the wiring material. Also, the melting point of Cu is 1083° C and is high in comparison to 660° C of Al; and it is said that generally electromigration (EM) resistance is high and even the reliability is excellent.

[0003]

In the case where Cu wiring is formed, fabrication by dry etching is difficult; and therefore, a damascene process is generally used. The damascene process is a method that forms Cu wiring by making grooves for the wiring on an insulative film formed on a semiconductor substrate, filling Cu into the grooves, and polishing excess Cu other than the Cu filled into the wiring grooves.

[0004]

Also, to use Cu as the wiring material, it is necessary to provide a barrier metal film around the Cu for preventing diffusion of the Cu into the insulative film and corrosion of the Cu. Hereinafter, the current generally-used manufacturing method of a semiconductor device having Cu wiring is described with reference to the drawings.

[0005]

First, the conventional manufacturing method of a semiconductor device illustrated in Fig. 9 is described. Fig. 9a illustrates lower layer wiring on which upper layer wiring is formed. The lower layer wiring portions also are formed using a process similar to the upper layer wiring recited below.

[0006]

An insulative film 1b is formed on the lower layer wiring (Fig. 9b); and subsequently, wiring grooves and wiring holes are formed in the insulative film by lithography and anisotropic etching (Fig. 9c). Subsequently, a barrier metal film 3b which is a conductive film is formed (Fig. 9d), and Cu 4b is filled (Fig. 9e).

[0007]

Next, excess Cu and the barrier metal film 3b other than that of the wiring grooves or the wiring holes are removed by chemical mechanical polishing (CMP) (Fig. 9f); and a barrier insulative film 8b which is an insulator is formed (Fig. 9g). Thus, a Cu wiring structure that is covered on a lower face and side faces by the barrier metal film 3b, which is a conductor, and on an upper face by the barrier insulative film 8b, which is an insulator, is formed.

[0008]

Here, it is reported in patent reference 1 that in the case where a width of the wiring (wiring groove) is at least 7 times a via (also referred to as "wiring hole" and "connection hole") diameter, lead breakage defects occur due to the creation of voids (cavities) below the vias and in the vias; and lead breakage defects accelerate most around 150° C. Similarly, it is reported also in non-patent reference 1 that in the case where lower layer wiring connected by vias are wide, voids occur at the lower layer wiring surface forming the connection portion; and lead breakage defects accelerate most during constant temperature storage at 190° C.

[0009]

Next, a manufacturing method of the conventional semiconductor device illustrated in Fig. 10 is described. Fig. 10 illustrates a formation method of copper alloy wiring in the case where an alloy sputter target is used as indicated in patent reference 2 and the like. Fig. 10a illustrates lower layer wiring on which upper layer wiring is formed. The lower layer wiring portion also can be formed using a process similar to that of the upper layer recited below.

[0010]

The insulative film 1b is formed on the lower layer wiring (Fig. 10b); and subsequently, wiring grooves and wiring holes are formed in the insulative film 1b by lithography and anisotropic etching (Fig. 10c). Subsequently, a barrier metal film 3b which is a conductive film is formed. Further, an alloy seed layer 10b forming an electrode for when the wiring grooves and the wiring holes are filled is formed by

sputtering using a Cu alloy target (Fig. 10d). Subsequently, Cu 4b is filled by a plating process or chemical vapor deposition (CVD) (Fig. 10e).

[0011]

Then, the added element in the alloy seed layer 10b is diffused into the Cu 4b by heat treatment, and the Cu 4b is alloyed (Fig. 10f). Then, excess Cu alloy 6c and the barrier metal film 3b other than those of the wiring grooves and the wiring holes are removed by CMP (Fig. 10g); and a barrier insulative film 8b which is an insulator is formed (Fig. 10h). Thus, a Cu wiring structure that is covered on a lower face and side faces by the barrier metal film 3b, which is a conductor, and on an upper face by the barrier insulative film 8b, which is an insulator, is formed.

[0012]

Also, patent reference 3 describes the case where a CuSn alloy seed layer is used when forming metal wiring of a semiconductor device.

[Patent Reference 1]

Japanese Published Unexamined Patent Application No. 2001-298084

[Patent Reference 2]

Japanese Published Unexamined Patent Application No. 2000-150522

[Patent Reference 3]

Japanese Published Unexamined Patent Application No. 2000-208517

[Non-patent Reference 1]

Stress-Induced Voiding Under Vias Connected to Wide Cu Metal Leads, Proceeding of IEEE International Reliability Physics Symposium 2002, USA, The Electron Device Society and The Reliability Society of the Institute of Electrical and Electronics Engineers, Inc, published April 7, 2002, p. 312-321.

[0013]

[Problem to be Solved by the Invention]

Regarding the reliability of Cu wiring formed as illustrated in Fig. 9, EM resistance and also void formation due to stress induced migration (SM) are becoming important problems. Tensile stress applied to Cu wiring portions, which occur due to

differences in the coefficients of thermal expansion of Cu and the insulative film, become the driving force of void formation.

[0014]

Conversely, as discussed in patent reference 1 recited above and non-patent reference 1 recited above, lead breakage defects occur due to void formation. It can be expected that defects caused by such stress will become even more prominent when via diameters are further reduced due to element miniaturization.

[0015]

Also, as a countermeasure for EM and SM, heretofore, many alloys of Cu wiring have been studied. In alloying, the migration resistance of Cu can be increased by changing the metal composition of Cu.

[0016]

However, as in patent reference 3 recited above, Cu alloy wiring formed by the method illustrated in Fig. 10 have problems such as those hereinafter. In other words, in the case where the alloy seed layer 10b is formed, Cu alloy is formed by diffusing the added element in the alloy seed layer 10b into the Cu 4b by heat treatment. On the other hand, the added element in the alloy seed layer 10b diffuses into the Cu 4b by the heat treatment; and a portion precipitates into a crystal grain boundary 7b of a Cu crystal grain 6c; but much remains in the Cu crystal grain 6c. Electron scattering occurs due to the effects of the added element remaining in the Cu crystal grain 6c.

[0017]

Also, the resistivity of the formed Cu alloy wiring unfortunately increases due to the effects of the grain boundary scattering of electrons due to the smaller Cu crystal grains caused by the heat treatment.

[0018]

Also, it is acceptable in the case where the added element in the alloy seed layer 10b uniformly diffuses into the Cu 4b by the heat treatment; but in the case where the diffusion speed of the added element into the Cu 4b is slow, much of the added element remains in the alloy seed layer 10b even after the heat treatment is performed. In this

case, due to the effects of much of the added element remaining in the alloy seed layer 10b, the resistivity of the Cu wiring increases, and also becomes unstable for the thermal cycle during multiple layer wiring formation because the concentration profile of the added element may change further in the bulk Cu 6c due to the heat treatment for forming the wiring of the upper layer.

[0019]

Further, the growth of the Cu 6c crystal grains is inhibited by the effects of the added element in the alloy seed layer 10b. Particularly in such a case as where the added element precipitates in the Cu crystal grain boundary, pinning occurs at the grain boundary due to the effects of the precipitated added element; and the Cu crystal grain growth of the heat treatment is inhibited. As a result, the Cu crystal grain diameter becomes smaller; and therefore, the resistivity of the Cu wiring is increased while also affecting the wiring reliability of EM, SM, etc.

[0020]

Also, in the case where the Cu alloy seed layer 10b is formed by sputtering, the filling properties of Cu by sputtering are different according to the width of wiring grooves and wiring holes, and therefore discrepancies occur. In other words, filling properties by sputtering worsen for fine wiring; and therefore, the film thickness of the alloy seed layer 10b that accumulates on the bottom of the wiring grooves becomes thin. Therefore, for fine wiring grooves, the concentration of the added element in the wiring grooves becomes relatively small in comparison to that of wide wiring grooves. As a result, the resistivity of the Cu wiring for fine wiring grooves becomes lower in comparison to that of wide wiring grooves. Thus, in the case where the alloy seed layer 10b is formed by sputtering, the concentration of the added element is different according to the width of the wiring grooves; and therefore, the resistivity of the Cu wiring varies with the width of the wiring grooves.

[0021]

Further, it is reported in patent reference 3 recited above that in the case where a CuSn alloy seed layer is used, the adhesion between the barrier metal film and the alloy

seed layer worsens. Thus, ensuring the adhesion between the barrier metal film 3b and the alloy seed layer 10 is also an important problem.

[0022]

The present invention was conceived in consideration of the circumstances recited above, and is directed to improve the circuit delay and provide a metal for wiring having high performance, excellent SM resistance and EM resistance, and high reliability; a semiconductor device using the metal for wiring; and a manufacturing method therfor.

[0023]

[Means for Solving the Problem]

To solve the problems recited above, the present invention includes a metal for wiring that contains a multicrystal having Cu (copper) as a main component and an added element other than Cu, characterized in that a concentration of the added element at a crystal grain boundary and a crystal grain boundary proximity of a crystal grain of the multicrystal is higher than that of the crystal grain interior.

[0024]

According to this aspect, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form a diffusion path of SM and EM of the metal for wiring; and thereby, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved. Further, by the present invention, the circuit delay can be improved; and a high performance metal for wiring can be provided.

[0025]

The metal for wiring of the present invention recited above is characterized in that the added element is an element of at least any one of Ti (titanium), Zr (zirconium), Hf (hafnium), Cr (chromium), Co (cobalt), Al (aluminum), Sn (tin), Ni (nickel), Mg (magnesium), and Ag (silver).

[0026]

According to this aspect, a predetermined element, having a solid solubility limit in

Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added to a metal for wiring having Cu as the main component; and therefore, the added element can be introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity recited above. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved.

[0027]

The metal for wiring of the present invention recited above is characterized in that the crystal grain boundary and the crystal grain boundary proximity are formed of an intermetallic compound between Cu and an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[0028]

According to this aspect, a stable intermetallic compound is formed at the Cu crystal grain boundary and the crystal grain boundary proximity (outermost surface of the Cu crystal grain) which form the diffusion path for SM and EM; and thereby, the migration of Cu along the Cu crystal grain boundary is inhibited; and the reliability of the metal for wiring is improved.

[0029]

The metal for wiring of the present invention recited above is characterized in that the crystal grain boundary and the crystal grain boundary proximity contain an oxide of an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[0030]

According to this aspect, a stable metallic oxide is formed at the Cu crystal grain boundary and the crystal grain boundary proximity (outermost surface of the Cu crystal grain) which form the diffusion path for SM and EM; and thereby, the migration of Cu along the Cu crystal grain boundary is inhibited; and the reliability of the metal for wiring is improved.

[0031]

The metal for wiring of the present invention recited above is characterized in that a

concentration of the added element of the crystal grain interior is at most 0.1 atomic %.

[0032]

According to this aspect, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form the diffusion path for SM and EM; and on the other hand, a configuration is formed in which the crystal grain interior contains an ultra trace amount of the added element of at most 0.1 atomic %; and thereby, the migration of Cu along the Cu crystal grain boundary is inhibited; and the reliability of the metal for wiring is improved.

[0033]

To solve the problems recited above, the present invention comprises a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, characterized in that the metal wiring comprises the metal for wiring described above.

[0034]

According to this aspect, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form the diffusion path for SM and EM of the metal wiring of the semiconductor device; and thereby, the migration of Cu along the Cu crystal grain boundary is inhibited; and the reliability of the metal wiring can be improved. Further, by the present invention, the circuit delay can be improved; and a semiconductor device can be provided having high performance metal wiring.

[0035]

To solve the problems recited above, the present invention includes a manufacturing method of a metal for wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu, comprising: a Cu multicrystal formation step that forms the multicrystal comprising Cu as a main component; an added element layer formation step that forms a layer comprising the added element on the Cu multicrystal; and an added element diffusion step that diffuses

the added element into the Cu multicrystal.

[0036]

According to this aspect, Cu crystal grains are grown in the Cu multicrystal formation step, and an added element is introduced into the Cu multicrystal; and therefore, inhibition of the Cu crystal grain growth due to the effects of an added element during heat treatment, such as that seen in the case where a Cu alloy seed layer is formed in a film using a sputter target having a mixture of several % of the added element, does not occur. Also, almost none of the added element exists in the bulk Cu; and therefore, electron scattering in the bulk Cu due to the added element can be inhibited; and the resistance of the Cu metal for wiring can be reduced. As a result, the circuit delay can be improved; and a metal for wiring can be provided having high performance, excellent SM resistance and EM resistance, and high reliability.

[0037]

The manufacturing method of a metal for wiring of the present invention recited above is characterized in that a heating step that heats the substrate having the formed Cu multicrystal, the added element layer formation step, and the added element diffusion step are performed simultaneously.

[0038]

According to this aspect, in addition to the effects described above, these steps are performed simultaneously, thereby omitting steps and enabling easier manufacturing of the metal for wiring.

[0039]

The manufacturing method of a metal for wiring of the present invention recited above is characterized in that the added element is an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[0040]

According to this aspect, a predetermined element, having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added to a metal for wiring having Cu as the main component; and

therefore, the added element can be introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved.

[0041]

To solve the problems recited above, the present invention comprises a manufacturing method of a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, comprising: a Cu multicrystal formation step that forms the multicrystal comprising Cu as a main component; an added element layer formation step that forms a layer comprising the added element on the Cu multicrystal; and an added element diffusion step that diffuses the added element into the Cu multicrystal.

[0042]

According to this aspect, Cu crystal grains are grown in the Cu multicrystal formation step, and an added element is introduced into the Cu multicrystal; and therefore, inhibition of the Cu crystal grain growth due to the effects of an added element during heat treatment, such as that seen in the case where a Cu alloy seed layer is formed in a film using a sputter target having a mixture of several % of the added element, does not occur. Also, almost none of the added element exists in the bulk Cu; and therefore, electron scattering in the bulk Cu due to the added element can be inhibited; and the resistance of the Cu wiring of the semiconductor device can be reduced. As a result, the circuit delay can be improved; and a semiconductor device can be provided including metal wiring having high performance, excellent SM resistance and EM resistance, and high reliability.

[0043]

The present invention that solves the problems recited above comprises a manufacturing method of a semiconductor device comprising metal wiring that contains a multicrystal comprising Cu as a main component and an added element other

than Cu on a substrate comprising a formed semiconductor element, comprising: an insulative film formation step that forms an insulative film on the substrate; a wiring recess formation step that forms a recess for wiring comprising at least either of a groove or a hole in the insulative film; a Cu film formation step that forms Cu in a film to fill the wiring recess; an excess Cu removal step that removes excess Cu other than Cu filled into the wiring recess by chemical mechanical polishing; an added element layer formation step that forms a layer comprising the added element on the Cu formed in a film; an added element diffusion step that diffuses the added element into Cu formed in a film; and an excess added element removal step that removes an excess added element from the added element layer.

[0044]

According to this aspect, Cu crystal grains are grown in a step that forms the Cu multicrystal, and an added element is introduced into the Cu multicrystal. Therefore, inhibition of the Cu crystal grain growth due to the effects of an added element due to heat treatment, such as that seen in the case where a Cu alloy seed layer is formed in a film using a sputter target having a mixture of several % of the added element, does not occur. Also, almost none of the added element exists in the bulk Cu (Cu crystal grain interior); and therefore, electron scattering due to the added element in the bulk Cu is inhibited; and the resistance of the Cu wiring of the semiconductor device can be reduced. Further, according to the present invention, the added element is introduced (diffused into the Cu) from the upper layer after the Cu is filled; and therefore, it becomes difficult for differences to occur in the concentrations of the added element due to different filling properties of Cu among the grooves and the holes as seen in the case where a Cu alloy seed layer is formed in a film using a sputter target and the wiring grooves and the wiring holes are filled with Cu. As a result, variation of the resistivity of the Cu wiring according to the width of the wiring grooves is eliminated.

[0045]

The present invention that solves the problems recited above comprises a manufacturing method of a semiconductor device comprising metal wiring that

contains a multicrystal comprising Cu as a main component and an added element other than Cu on a substrate comprising a formed semiconductor element, comprising: an insulative film formation step that forms an insulative film on the substrate; a wiring recess formation step that forms a recess for wiring comprising at least either of a groove or a hole in the insulative film; a barrier metal film formation step that forms a barrier metal film, that prevents a diffusion of Cu, on the insulative film comprising the wiring recess; a Cu film formation step that forms Cu in a film to fill onto the barrier metal film of the wiring recess; an excess Cu removal step that removes excess Cu other than Cu filled into the wiring recess by chemical mechanical polishing; a barrier metal film removal step that removes excess of an excess barrier metal film other than a barrier metal film filled into the wiring recess by chemical mechanical polishing; an added element layer formation step that forms a layer comprising an added element on the Cu formed in a film; an added element diffusion step that diffuses the added element into Cu formed in a film; and an excess added element removal step that removes an excess added element from the added element layer.

[0046]

According to this aspect, Cu crystal grains are grown in a Cu multicrystal formation step, and an added element is introduced into the Cu multicrystal; and therefore, inhibition of the Cu crystal grain growth due to the effects of an added element during heat treatment does not occur. Also, almost none of the added element exists in the bulk Cu; and therefore, electron scattering due to the added element in the bulk Cu is inhibited; and the resistance of the Cu wiring of the semiconductor device can be reduced. Also, the added element is introduced from the upper layer after the Cu is filled; and therefore, it becomes difficult for differences to occur in the concentrations of the added element in the Cu wiring; and variation of the resistivity of the Cu wiring according to the width of the wiring grooves is eliminated. Further, a barrier metal film is provided between the Cu and the insulative film; and therefore, the diffusion of the Cu into the insulative film and the corrosion of the Cu are prevented.

[0047]

The manufacturing method of a semiconductor device of the present invention recited above is characterized in that the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed prior to the excess Cu removal step.

[0048]

According to this aspect, a stable intermetallic compound can be formed between the Cu and the added element at the Cu crystal grain boundary and the crystal grain boundary proximity; and thereby, the EM resistance and SM resistance are improved; and the reliability of the wiring of the semiconductor device increases.

[0049]

The manufacturing method of a semiconductor device of the present invention recited above is characterized in that the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed after the excess Cu removal step.

[0050]

According to this aspect, the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed after the excess Cu removal step; and thereby, a stable intermetallic compound is formed between the Cu and the added element on the Cu crystal grain surface contacting the layer formed on the Cu which is the metal for wiring. As a result, the adhesion between the Cu which is the metal for wiring and the upper layer improves; and the reliability of the wiring of the semiconductor device increases.

[0051]

The manufacturing method of a semiconductor device of the present invention recited above is characterized in that a heating step that heats the substrate, the added element layer formation step, and the added element diffusion step are performed simultaneously.

[0052]

According to this aspect, in addition to the effects described above, these steps are

performed simultaneously, thereby omitting steps and enabling easier manufacturing of the semiconductor device.

[0053]

The manufacturing method of a semiconductor device of the present invention recited above is characterized in that the added element is an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag.

[0054]

According to this aspect, a predetermined element, having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added into metal wiring of a semiconductor device having Cu as the main component; and therefore, the added element can be introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal wiring of the semiconductor device can be improved.

[0055]

[Embodiments of the Invention]

Next, exemplary embodiments of the present invention are described in detail with reference to the drawings.

[0056]

(First Exemplary Embodiment)

A Cu wiring structure of a semiconductor device according to a first exemplary embodiment of the present invention is described with reference to Fig. 1.

[0057]

A Cu wiring structure of a semiconductor device illustrated in Fig. 1 includes wiring of a lower layer formed of an insulative film 1a, a barrier metal film 3a, Cu 4a, and a barrier insulative film 8a; and wiring of an upper layer formed of an insulative film 1b, a barrier metal film 3b, a Cu crystal grain 6b, a Cu crystal grain boundary and proximity thereof 7b, and a barrier insulative film 8b. The Cu 4a of the wiring of the lower layer has a similar configuration to the Cu crystal grain 6b and the Cu crystal

grain boundary and proximity thereof 7b of the wiring of the upper layer.

[0058]

Also, the first exemplary embodiment is characterized by a structure in which much of at least one of an added element, an intermetallic compound formed of Cu and an added element, or an oxide of an added element precipitates at the grain boundary of the Cu crystal grain 6b and proximity thereof, and at the interface and proximity thereof between the Cu crystal grain 6b and the barrier metal film 3b (indicated by 7b).

[0059]

Cu metal wiring is formed of a multicrystal of Cu in which a metal element other than Cu is added. The Cu crystal grain 6b having a multicrystal configuration has uninhibited crystal grain growth and is formed of Cu crystal grains having average and moderate sizes of about 1 μm to 10 μm.

[0060]

Also, the Cu crystal grain boundary 7b and the interface 7b between the Cu crystal grain 6b and the barrier metal film 3b have a structure in which an added element or a compound including an added element (such as an intermetallic compound or oxide of Cu) precipitates. Further, the structure is characterized in that, in addition to the Cu crystal grain boundary and the like, intermetallic compounds of the added element and Cu, and the like are formed in the Cu crystal grain boundary proximity 7b. The Cu crystal grain boundary proximity recited herein indicates a location about 10 nm into the interior from the crystal grain surface of the Cu crystal grain 6b.

[0061]

The concentration of the added element of the grain boundary of the Cu crystal grain 6b and the grain boundary proximity 7b is not particularly limited; but an added element exists in the grain boundary of the Cu crystal grain 6b and the grain boundary proximity 7b at least more plentifully than in the Cu crystal grain 6b interior. Specifically, the concentration of the added element of the grain boundary of the Cu crystal grain 6b and the grain boundary proximity 7b is about 2 - 1000 times the concentration of the added element in the Cu crystal grain 6b interior, and favorably

about 10 - 100 times thereof.

[0062]

The added element concentration of the Cu crystal grain boundary and proximity thereof 7b may be measured by, for example, X-ray spectroscopy. This measurement method can detect the added element concentration of the Cu crystal grain boundary and proximity thereof 7b if the concentration is at least 0.1 atomic %.

[0063]

On the other hand, the Cu crystal grain interior 6b, in other words, the bulk Cu 6b, has only an amount of at most 0.1 atomic % of the added element, and is in a state of nearly pure Cu. The Cu crystal grain interior recited herein is a portion that excludes the Cu crystal grain boundary proximity described above from the Cu crystal grain.

[0064]

The added element concentration of the Cu crystal grain interior 6b can be measured by, for example, Secondary Ion Mass Spectroscopy (SIMS), X-ray spectroscopy, and the like. SIMS can be used in the case where the Cu crystal grain diameter to be measured is large in comparison to the beam diameter (normally several tens of μm) used in SIMS. In the case where the Cu crystal grain diameter is smaller than this, an average concentration in the crystal grain boundary and the Cu crystal grain interior can be ascertained by SIMS; the added element concentration of the Cu crystal grain boundary and the grain boundary proximity 7b described above can be ascertained; and thereby, the added element concentration of the Cu crystal grain interior can be inferred. Also, the added element concentration, if at least 1 atomic %, can be measured by X-ray spectroscopy from the Cu crystal surface. The detection sensitivity by X-ray spectroscopy is about 0.1 atomic %.

[0065]

Thus, the location of the grain boundary of the Cu crystal grain and the grain boundary proximity 7b has a configuration having a concentration (content) of the added element that is higher than that of the Cu crystal grain interior 6b.

[0066]

Also, an added element having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient in the Cu crystal grain boundary is used. The diffusion coefficient of the added element in the Cu bulk may not be high. For the added element, it is particularly favorable to use titanium (Ti), zirconium (Zr), hafnium (Hf), chromium (Cr), and cobalt (Co). Additionally for the added element, aluminum (Al), tin (Sn), nickel (Ni), magnesium (Mg), and silver (Ag) may be used.

[0067]

For such Cu wiring structure, problems do not occur wherein the resistivity of the Cu wiring increases due to the effects of electron scattering due to an added element remaining in the bulk Cu 6c of the conventional art and due to the effects of grain boundary scattering of electrons due to size reductions of the crystal grain. Also, by such a structure of the Cu metal wiring, the electron scattering due to the added element in the bulk Cu 6b can be inhibited; and the transfer delay of the wiring can be improved. Also, in the Cu crystal grain boundary and crystal grain interface proximity thereof 7b forming the diffusion path of Cu of void formation, an added element or a compound including an added element precipitates; and thereby, the diffusion of the Cu is inhibited.

[0068]

Further, in the case where an easily oxidizable element having a higher reducibility than Cu is used as the added element, and even supposing that the Cu metal wiring is exposed to oxygen or water vapor, the added element existing in the grain boundary oxidizes first; and the oxidized added element serves as a barrier that prevents oxidation of the Cu; and therefore, effects of oxidation prevention and corrosion prevention of the Cu are provided. Also, forming a layer of an easily oxidized element having a higher reducibility than that of the Cu on the Cu surface provides an effect that inhibits oxidation of the Cu during heat treatment and a gettering effect of oxygen and impurities existing in the Cu crystal grain surface and the Cu crystal grain interior.

[0069]

At this point, it is indicated that, regarding EM as a migration path of the Cu which becomes a reliability problem of Cu wiring, diffusion at the interface between the Cu crystal grain and the barrier insulative film or the Cu crystal grain boundary is more dominant than the diffusion in the bulk Cu in non-patent reference 2 ("Electromigration path in Cu thin-film lines," Applied Physics Letters, USA, American Institute of Physics, published May 17, 1999, Vol. 74, p. 2945-2947), and the like.

[0070]

Also, regarding SM as well, voids may be formed in the crystal grain boundary by SM; and therefore, it may be considered that the Cu crystal grain boundary forms a diffusion path. Therefore, it may be considered that inhibition of interface/grain boundary diffusion is important for improvement of the reliability of the Cu metal wiring. Accordingly, it may be considered that the improvement of the reliability of the Cu metal wiring by alloying is because the added impurity element precipitates at the interface between the Cu crystal grain and another layer or in the Cu crystal grain boundary, thereby inhibiting diffusion of the Cu via the interface between the Cu crystal grain and another layer and via the Cu crystal grain boundary.

[0071]

The present invention inhibits alloying of the bulk Cu, inhibits a resistance increase of the Cu wiring by introducing an added element only to the interface between the Cu crystal grain and another layer and to the Cu crystal grain boundary, and realizes a provision of highly reliable Cu metal wiring having EM and SM resistance.

[0072]

Next, a manufacturing method of a semiconductor device having Cu wiring of the first exemplary embodiment is described with reference to Fig. 2.

[0073]

Fig. 2a illustrates lower layer wiring on which upper layer wiring is formed. The lower layer wiring portion also is formed using a process similar to that of the upper layer wiring recited below.

[0074]

An insulative film 1b is formed on the lower layer wiring (Fig. 2b); and subsequently, wiring grooves and wiring holes are made in the insulative film 1b by lithography and anisotropic etching (Fig. 2c). Subsequently, a barrier metal film 3b is formed in the wiring grooves and the wiring holes that were made, and Cu 4b is filled (Fig. 2d). Then, heat treatment is performed for grain growth of Cu (Fig. 2e). The heat treatment is performed at a low temperature of at most 400° C. Favorably, it is at most 300° C. The heat treatment for Cu grain growth also may be omitted.

[0075]

Subsequently, a layer 5b of an element to be added to the Cu crystal is formed on the Cu 4b surface (Fig. 2f). Then, heat treatment is performed for diffusing the added element 5b into the Cu crystal 4b (Fig. 2g). The temperature of the heat treatment is set to 300° C to 500° C; and the time is set to 10 minutes to one hour.

[0076]

Then, the excess added element layer 5b is removed by wet etching (Fig. 2h). To remove the added element layer 5b, CMP may be used in lieu of wet etching. Then, the excess Cu 6b and barrier metal film 3b other than that of the wiring grooves and the wiring holes are removed by CMP (Fig. 2i). Then, a barrier insulative film 8b that prevents corrosion and diffusion of the Cu is formed on the entire surface (Fig. 2j).

[0077]

By repeating Figs. 2b to j, further wiring of the upper layer can be formed.

[0078]

In the manufacturing method hereinbefore, the formation of the added element layer 5b (Fig. 2f) and the diffusion of the added element into the Cu multicrystal (Fig. 2g) are performed separately; but by forming the added element layer 5b at a high temperature, it is also possible to simultaneously perform the formation of the added element layer 5b and the diffusion of the added element into the Cu multicrystal. By simultaneously performing the two steps, the number of steps can be reduced; and a semiconductor device having Cu wiring can be more easily manufactured. The temperature and time in the case where the two steps are thus performed simultaneously may be similar to

those of the heat treatment for diffusing the added element into the Cu crystal. This is similar also for the exemplary embodiments described hereinafter.

[0079]

Also, in this exemplary embodiment, the Cu is filled after the barrier metal film 3b is formed; but the barrier metal film 3b is not an essential configuration, and may not be formed. By forming the barrier metal film 3b, the Cu 6b can be inhibited from diffusing into the insulative film 1b.

[0080]

Also, the description hereinbefore uses a dual damascene process that simultaneously makes wiring grooves and wiring holes; but implementation is similar also for a wiring layer formation in the case where a single damascene process that makes only wiring grooves or only wiring holes is used. In the present invention, wiring grooves and wiring holes are also generally referred to as "wiring recesses."

[0081]

(Second Exemplary Embodiment)

A Cu wiring structure of a semiconductor device according to a second exemplary embodiment of the present invention is described with reference to Fig. 3.

[0082]

In the Cu wiring structure illustrated in Fig. 3, in addition to the structure of the first exemplary embodiment, a stable intermetallic compound layer between Cu and an added element is formed at the interface between the barrier insulative film 8b and the Cu crystal grain 6b. Therefore, the adhesion between the Cu 6b, which is a metal for wiring, and the barrier insulative film 8b, is improved; and the reliability of the wiring improves.

[0083]

Next, the manufacturing method of the semiconductor device having Cu wiring of the second exemplary embodiment is described with reference to Fig. 4.

[0084]

The manufacturing method of the second exemplary embodiment is different from

that of the first exemplary embodiment by the point that the added element layer 5b is formed after removing the excess Cu 6b and the excess barrier metal 3b by CMP, but is otherwise similar.

[0085]

Fig. 4a illustrates lower layer wiring on which upper layer wiring is formed. The lower layer wiring portion also can be formed using a process similar to that of the upper layer wiring recited below.

[0086]

An insulative film 1b is formed on the lower layer wiring (Fig. 4b), and subsequently, wiring grooves and wiring holes are made in the insulative film 1b by lithography and anisotropic etching (Fig. 4c). Subsequently, a barrier metal film 3b is formed, and Cu 4b is filled (Fig. 4d). Next, heat treatment is performed for crystal grain growth of the filled Cu (Fig. 4e). The heat treatment is performed at a low temperature of at most 400° C. Favorably, it is at most 300° C. The heat treatment for Cu grain growth also may be omitted.

[0087]

Subsequently, the excess Cu and the excess barrier metal other than that of the wiring grooves and the wiring holes are removed by CMP (Fig. 4f). Then, a layer 5b of an element to be added to the Cu is formed on the Cu surface (Fig. 4g). Then, heat treatment is performed for diffusing the added element into the Cu (Fig. 4h). The temperature of the heat treatment is set to about 300° C to 500° C; and the time is set to about 10 minutes to one hour.

[0088]

Then, the excess added element layer 5b is removed by wet etching (Fig. 4i). To remove the added element layer 5b, CMP may be used in lieu of wet etching. Then, a barrier insulative film 8b that prevents corrosion and diffusion of the Cu is formed on the entire surface (Fig. 4j).

[0089]

By repeating Figs. 4b to j, further wiring of the upper layer can be formed.

[0090]

In the manufacturing method hereinbefore, the formation of the added element layer 5b (Fig. 4g) and the diffusion of the added element into the Cu multicrystal (Fig. 4h) are performed separately; but by forming the added element layer 5b under high temperature conditions, it is also possible to simultaneously perform the formation of the added element layer 5b and the diffusion of the added element into the Cu multicrystal. By simultaneously performing the two steps, the number of steps can be reduced; and a semiconductor device having Cu wiring can be more easily manufactured.

[0091]

Also, the description hereinbefore uses a dual damascene process that simultaneously makes wiring grooves and wiring holes; but implementation is similar also for making a wiring recess in the case where a single damascene process that makes only wiring grooves or only wiring holes is used.

[0092]

(Third Exemplary Embodiment)

A Cu wiring structure of a semiconductor device according to a third exemplary embodiment of the present invention is described with reference to Fig. 5.

[0093]

The structure of the third exemplary embodiment illustrated in Fig. 5 is different from the structure of the second exemplary embodiment by the point that a barrier insulative film 8b is not used. In the third exemplary embodiment, a stable intermetallic compound layer is formed on the Cu surface; and thereby, oxidation and corrosion of the Cu is prevented; and therefore, the barrier insulative film 8b is unnecessary. By not providing the barrier insulative film 8b, the effective dielectric constant of the Cu wiring can be reduced; and therefore, the delay of the transfer is improved.

[0094]

Next, the manufacturing method of the semiconductor device having Cu wiring of

the third exemplary embodiment is described with reference to Fig. 6.

[0095]

Fig. 6a illustrates lower layer wiring on which upper layer wiring is formed. The lower layer wiring portion also can be formed using a process similar to that of the upper layer wiring recited below.

[0096]

An insulative film 1b is formed on the lower layer wiring (Fig. 6b); and subsequently, wiring grooves and wiring holes are made in the insulative film 1b by lithography and anisotropic etching (Fig. 6c). Subsequently, a barrier metal film 3b is formed, and Cu 4b is filled (Fig. 6d). Then, heat treatment is performed for Cu crystal grain growth (Fig. 6e). The heat treatment is performed at a low temperature of at most 400° C. Favorably, it is at most 300° C. The heat treatment for Cu grain growth also may be omitted.

[0097]

Subsequently, the excess Cu and barrier metal other than that of the wiring grooves and the wiring holes are removed by CMP (Fig. 6f). Then, a layer 5b of an element to be added to the Cu is formed on the Cu surface (Fig. 6g). Then, heat treatment is performed for diffusing the added element into the Cu (Fig. 6h). The temperature of the heat treatment is set to 300° C to 500° C; and the time is set to 10 minutes to one hour.

[0098]

Then, the excess added element layer 5b is removed by wet etching (Fig. 6i). To remove the added element layer 5b, CMP may be used in lieu of wet etching.

[0099]

By repeating Figs. 6b to i, further wiring of the upper layer can be formed.

[0100]

In the manufacturing method hereinbefore, the formation of the added element layer 5b (Fig. 6g) and the diffusion of the added element into the Cu multicrystal (Fig. 6h) are performed separately; but by forming the added element layer 5b at a high

temperature, it is also possible to simultaneously perform the formation of the added element layer 5b and the diffusion of the added element into the Cu multicrystal. By simultaneously performing the two steps, the number of steps can be reduced; and a semiconductor device having Cu wiring can be more easily manufactured.

[0101]

Also, the description hereinbefore uses a dual damascene process that simultaneously makes wiring grooves and wiring holes; but implementation is similar also for making a wiring recess in the case where a single damascene process that makes only wiring grooves or only wiring holes is used.

[0102]

[Example]

An example of the present invention is described hereinafter using Fig. 7 and Fig. 8.

[0103]

(Example)

Fig. 7 and Fig. 8 are cross-sectional views illustrating a manufacturing method of a semiconductor device of the example of the present invention.

[0104]

A 1000 nm SiO_2 film (insulative film) 1a was formed on a silicon substrate (not illustrated); a first wiring layer (wiring grooves) was made thereupon by a single damascene process; and then, a second wiring layer (wiring grooves) and connection holes (wiring holes) communicating with the first wiring layer were made on an upper portion thereof by a dual damascene process. The details are described hereinafter.

[0105]

An SiC film (stopper insulative film) 2a having a thickness of 50 nm, which is an etching stopper, was formed on the SiO_2 film 1a (Fig. 7a); then, an SiO_2 film (insulative film) 1b having a thickness of 350 nm, that insulates between wiring of the first wiring layer, was formed (Fig. 7b); and wiring grooves were formed in the SiO_2 film 1b by lithography and etching (Fig. 7c). Subsequently, a barrier metal film 3a formed of a TaN film and a Ta film and a 100 nm Cu thin film were formed by ionic sputtering on

the entire substrate surface; and using the Cu film as an electrode, Cu 4a was filled by an electroplating process (Fig. 7d).

[0106]

Then, heat treatment in a nitrogen atmosphere for Cu crystal grain growth was performed (Fig. 7e); and then a Ti film (added element layer) 5a having a film thickness of 20 nm was formed on the entire Cu surface by sputtering (Fig. 7f).

[0107]

Then, heat treatment in a nitrogen atmosphere at 350° C for 30 minutes was performed, and Ti was diffused into the Cu from the Cu surface (Fig. 7g). Here, the Ti diffuses via the Cu crystal grain boundary; and almost none diffuses into the bulk; and therefore, much Ti is included in the Cu crystal grain boundary proximity 7a; and a structure can be formed in which almost no Ti mixes into the bulk Cu 6a.

[0108]

Then, the excess Ti was removed by hydrofluoric acid; and then the excess Cu, Ta, and TaN layers were removed by CMP (Fig. 7h). An SiCN film (barrier insulative film) 8a having a thickness of 50 nm was formed on the entire surface by plasma CVD, and a first wiring layer was formed (Fig. 7i).

[0109]

Further, an SiO_2 film (insulative film) 1c, an SiC film (stopper insulative film) 2b, and an SiO_2 film (insulative film) 1d, having thicknesses of 400 nm, 50 nm, and 400 nm, respectively, were formed by plasma CVD (Fig. 7j); a portion of the SiO_2 film 1c, the SiC film 2b, and the SiO_2 film 1d was sequentially removed using the SiCN film 8a as an etching stopper by lithography and anisotropic dry etching; and the main portions of connection holes (wiring holes) between the first wiring layer -- 2 wiring layer were made (Fig. 7k). Then, a portion of the SiO_2 film 1c was removed and the main portions of the wiring grooves of a second wiring layer were formed by lithography and anisotropic etching using the SiC film 2b as an etching stopper (Fig. 8l). Then, the SiCN film 8a of the connection hole bottom portion between the first wiring layer -- second wiring layer and the SiC film 2b of the second wiring groove bottom portion

were removed by anisotropic etching; and the upper connection face of the first wiring layer was exposed (Fig. 8m).

[0110]

Then, a cleaning of the surface of the first wiring layer that was exposed at the bottom of the connection holes between the first wiring layer -- second wiring layer was performed by a slight etching of the surface by Ar ions in a vacuum apparatus.

[0111]

Then, while maintaining the vacuum, to coat the inner face of the wiring grooves of the second wiring layer and the connection holes between the first wiring layer -- second wiring layer, a barrier metal film 3b wherein a TaN film and a Ta film were laminated in this order and a 100 nm Cu thin film were formed by ionic sputtering by a procedure similar to that of the first wiring layer formation; and Cu 4b was filled by an electroplating process using the Cu thin film as a seed (Fig. 8n).

[0112]

Then, similar to the first wiring layer formation, heat treatment was performed in a nitrogen atmosphere for Cu crystal grain growth (Fig. 8o); and then a Ti film (added element layer) 5b having a film thickness of 20 nm was formed by sputtering on the entire Cu surface (Fig. 8p). Then, heat treatment was performed in a nitrogen atmosphere at 350° C for 30 minutes; and Ti was diffused into the Cu from the Cu surface (Fig. 8q).

[0113]

Then, the excess Ti was removed by hydrofluoric acid; and then the excess Cu, Ta, and TaN layers were removed by CMP (Fig. 8r). An SiCN film (barrier insulative film) 8b having a thickness of 50 nm was formed on the entire surface by plasma CVD; and further, an SiO_2 film 9 was formed as a cover film (Fig. 8s).

[0114]

After opening a junction portion in the cover film 9 communicating with the second wiring layer by lithography and etching, Ti, TiN, and Al films were sequentially formed by sputtering; and the Al/TiN/Ti laminated film was fabricated into a pad

pattern by lithography and etching for electrical measurement.

[0115]

(Comparison Example)

As a comparison example, a conventional semiconductor device having Cu wiring formed of upper layer and lower layer wiring was constructed as described in Fig. 9 described above. A substrate, an insulative film, a stopper insulative film, a barrier metal film, a barrier insulative film, and a cover insulative film were formed using similar materials, having similar thicknesses, and by similar formation methods as those of the example described above. Ti, which is the added element of the example, was not added.

[0116]

(Evaluation Result)

Fig. 11 illustrates the defect rate of samples, which were constructed according to the example and the comparison example having a connection hole diameter of 0.2 μm, a lower layer wiring (wiring groove) width of 10 μm, and via chains having a chain count (number of vias) of ten thousand, after each sample was stored at 150° C for 1000 hours.

[0117]

As a result of machining the samples by Focused Ion Beam (FIB) and observing the samples by Transmission Electron Spectroscopy (TEM), it was confirmed that the defects of the samples were lead breakage by void formation due to stress induced migration in the lower layer wiring portion 4a below the connection holes reported in patent reference 1 recited above.

[0118]

In the comparison example sample, open defects were prominent; and the defect rate increased with storage time. Also, it was confirmed that grain boundaries of Cu existed at the defect portions of the sample of the comparison example.

[0119]

On the other hand, in the sample of the example, the defects were drastically

improved. The defect occurrence rate of the example, when stored at 150° C for 1000 hours, was reduced to about one-fortieth of that of the comparison example. Furthermore, by optimizing the manufacturing steps, the defect occurrence was completely reduced even after storing for 1000 hours.

[0120]

Fig. 12 illustrates test results of electromigration resistance of connection holes (connection vias). Specifically, the cumulative failure probability by the failure time is illustrated. The test was performed at conditions of 300° C and a current density of 3.2 MA/cm^2; and a defect determination standard of a resistivity increase of 3% was used. It was confirmed that the sample of the example had an electromigration resistance of at least two times that of the sample of the comparison example.

[0121]

It may be considered that in the example, by introducing Ti into the Cu crystal grain boundary, the diffusion of the Cu via the grain boundary can be inhibited; and therefore, the stress induced migration resistance and the electromigration resistance improved.

[0122]

Fig. 13 is a plot of the change of the resistivity. Except for the formation of a Ta/TaN barrier metal film 3a on an SiO_2 insulative film 1a, and the further formation of a 700 nm Cu layer and the formation of a 20 nm Ti added element layer 5a, the samples used to measure the resistivity were blanket film samples constructed by a similar procedure as that of the exemplary embodiments recited above. In the blanket film samples, no wiring holes or wiring grooves were made. Fig. 13 illustrates the resistivities at each manufacturing stage for three samples, i.e., sample 1, sample 2, and sample 3. However, heat treatment was not performed after the Cu film formation and prior to the Ti film formation for the sample 1; heat treatment for Cu multicrystalization was performed after the Cu film formation and prior to the Ti film formation in a nitrogen atmosphere at 200 ° C for 30 minutes for the sample 2; and heat treatment for Cu multicrystalization is performed in a nitrogen atmosphere at 350° C for 30 minutes for the sample 3.

[0123]

The resistivity increase after performing the heat treatment for diffusing the Ti at 350° C for 30 minutes after Ti was formed in a film, in comparison to the resistivity after the heat treatment for Cu multicrystalization for the sample 3 having sufficient heat treatment after the Cu film formation, was reduced to less than 3% for all of the samples. Thus, the increase of the resistivity due to the Ti addition from the Cu surface was exceedingly small. This is because the Ti added from the surface diffuses along the Cu crystal grain boundary; and almost no Ti mixes into the Cu bulk.

[0124]

Fig. 14 illustrates measurement results of the distributions of Ti, Cu, and N in the Cu by secondary ion mass spectroscopy (SIMS) for a constructed blanket film sample described above. The horizontal axis of the graph of Fig. 14 represents the depth of the blanket film sample. Also, the vertical axis of the graph of Fig. 14 represents the secondary ion intensity measured by SIMS and corresponds to the number of atoms.

[0125]

A uniform concentration of Ti was detected in the depth direction in the Cu crystal. The diffusion coefficient of Ti in the bulk Cu at a temperature region of about 350° C was not high; and therefore it is not likely that Ti diffused into the bulk Cu to form the uniform distribution such as that of Fig. 14; and it may be considered that the Ti was added and uniformly diffused to the Cu bottom portion via the crystal grain boundary. Accordingly, it may be considered that almost no Ti mixed in the bulk Cu; and that Ti was localized in the grain boundary.

[0126]

Fig. 15 illustrates the relation of resistivity by differences in added elements and heat treatment. Except for the formation of a Ta/TaN barrier metal film 3a on an SiO_2 insulative film 1a, and the further formation of a 300 nm Cu layer and the formation of a Ni added element layer 5a, the samples used to measure the resistivity were blanket film samples constructed by a similar procedure as that of the exemplary embodiments recited above. In the blanket film samples, no wiring holes or wiring grooves were

made. The film thickness of the added element layer was set so that the added element Ni had an Ni concentration in the Cu of 3 atomic % when uniformly diffused into the Cu. The Ni was formed in a film by sputtering.

[0127]

Similarly, films were formed for each added element of Sn, Cr, and Co in lieu of the added element Ni; and each blanket film sample was constructed. Fig. 15 illustrates the resistivities for the blanket film samples having the added elements of Ni, Sn, Cr, and Co, respectively, at each stage of after the added element layer film formation, after the heat treatment in a nitrogen atmosphere at 350° C for 30 minutes, and after the heat treatment in a nitrogen atmosphere at 400° C for 30 minutes.

[0128]

Also for comparison, Fig. 15 illustrates the values of the resistivity of Cu having 1 atomic % concentration of the added element. The values are extracted from non-patent reference 3 (C. Kittel, translation supervised by Masao Doyama, "Kotai No Ryoshiron (Quantum Theory of Solids)," Maruzen Co., Ltd., published 1972, p. 338).

[0129]

As a result, regarding Sn and Ni, which form solid solutions easily in Cu, an increase of resistivity was seen as the heat treatment temperature increased. In particular, regarding Sn, when heat treatment was performed at a temperature of 400° C, an increase of the resistivity was seen at least the same as that of the case where it was uniformly mixed in the Cu at 1 atomic %. Conversely, regarding Cr and Co, which form precipitation alloys having low solid solubility limits into Cu, almost no increase of resistivity was seen as the heat treatment temperature increased. In the case where added elements such as Cr and Co, which form solid solutions easily in Cu, were used, the resistivity increased even when adding from the Cu surface. Accordingly, precipitation elements having low solid solubility limits into Cu are favorable as elements to add from the Cu surface.

[0130]

(Variations)

The metal for wiring of the semiconductor device and the manufacturing method thereof described hereinbefore may have variations such as those hereinafter.

[0131]

The exemplary embodiments recited above enable the lower layer wiring and the upper layer wiring to be formed by the same method; but the lower layer wiring and the upper layer wiring may be formed by different methods combining the exemplary embodiments recited above.

[0132]

For the constituent material of the insulative film 1, SiO_2 and the like, or another insulative material may be used. For the constituent material of the insulative film 1, it is favorable to use a material having a lower dielectric constant. The insulative film 1 may be formed by plasma CVD and the like. The film thickness of the insulative film 1 is not particularly limited; but the insulative film1a is about 100 - 3000 nm; the insulative film 1b is about 100 - 1000 nm; the insulative film1c is about 100 - 1000 nm; and the insulative film1d is about 100 - 1000 nm.

[0133]

For the constituent material of the stopper insulative film 2, an insulative material such as SiC, SiN, and SiCN may be used. For the constituent material of the stopper insulative film 2, it is favorable to use a material having a lower dielectric constant. The stopper insulative film 2 may be formed by plasma CVD and the like. The film thickness of the stopper insulative film 2 is not particularly limited; but the stopper insulative film 2a is about 10 - 100 nm; and the stopper insulative film 2b is about 10 - 100 nm. Also, the stopper insulative film 2 is used as an etching stopper of the wiring recess; but in the case where the wiring recess can be fabricated into the intended shape, the stopper insulative film 2 may not be used.

[0134]

The wiring grooves may be formed by lithography and etching (anisotropic etching) and the like. The width of the wiring grooves is not particularly limited, but may normally have a diameter of about 50 - 20000 nm.

[0135]

For the constituent material of the barrier metal film 3, a substance selected from a metal such as Ta, Ti, W, and the like; a nitride thereof; and a three element or four element nitride having Si and the like added thereto may be used. The barrier metal film 3 may be formed by ionic sputtering, CVD, Atomic Layer Deposition (ALD), and the like. The film thickness of the barrier metal film 3 is not particularly limited; but the barrier metal film 3a is about 5 - 50 nm; and the barrier metal film 3b is about 5 - 50 nm.

[0136]

For the formation method of the metal wiring Cu 4, a Cu thin film may be formed by ionic sputtering, CVD, metal organic chemical vapor deposition (MO-CVD), and the like; and then the metal wiring Cu 4 may be formed by an electroplating process using the Cu thin film as an electrode; or may be formed by MO-CVD. Also, it is possible to fill Cu into the wiring grooves by direct MO-CVD without forming the Cu thin film. The film thickness of the metal wiring Cu 4 is not particularly limited as long as it is formed enough to fill the wiring grooves and the wiring holes.

[0137]

The heat treatment for Cu crystal grain growth (Cu multicrystalization) may be performed under a reduction atmosphere such as nitrogen, hydrogen, and the like. The heat treatment may be performed at 400° C at most, and favorably at 300° C at most. This heat treatment step may be omitted.

[0138]

For the constituent material of the added element layer 5, Ti, Zr, Hf, Cr, Co, Al, Sn, Mg, Ag, and the like may be used. The added element layer 5 may be formed by sputtering and the like. The film thickness of the added element layer 5 is not particularly limited; but the added element layer 5a is about 5 - 100 nm; and the added element layer 5b is about 5 - 100 nm.

[0139]

The heat treatment for diffusing the added element into the Cu 4 from the added

element layer 5 may be performed under an atmosphere such as nitrogen. The heat treatment may be performed under the temperature conditions of about 300 - 500° C for 10 minutes to one hour.

[0140]

The removal of the excess added element layer 5 may be performed by wet etching by hydrofluoric acid, CMP, and the like.

[0141]

The removal of the excess Cu 4 and the excess barrier metal film 3may be performed by CMP and the like.

[0142]

For the constituent material of the barrier insulative film 8, an insulative material having a barrier property to Cu such as SiCN, SiC, and SiN may be used. The barrier insulative film 8 may be formed by plasma CVD and the like. The film thickness of the barrier insulative film 8 is not particularly limited; but the barrier insulative film 8a is about 20 - 100 nm; and the barrier insulative film 8b is about 20 - 100 nm.

[0143]

The wiring holes may be formed by lithography and anisotropic dry etching and the like. The width of the wiring hole is not particularly limited, but normally may have a diameter of about 50 - 1000 nm.

[0144]

For the constituent material of the cover insulative film 9, SiO_2 and the like, or another insulative material may be used. The cover insulative film 9 may be formed by plasma CVD and the like. The film thickness of the cover insulative film 9 is not particularly limited; but the cover insulative film 9 is about 100 - 10000 nm.

[0145]

In the exemplary embodiments and example hereinbefore, a semiconductor device, in which metal wiring formed of a metal for wiring containing a multicrystal having Cu as the main component and an added element other than Cu is formed on a substrate having a formed semiconductor element, was described as an example. For the

present invention, a metal for wiring having the structure described above and a metal for wiring manufactured by the manufacturing methods described above may be used not only for a semiconductor device, but also as a metal material for wiring of other applications.

[0146]

[Effects of the Invention]

As described hereinbefore, according to the metal for wiring of the present invention, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form a diffusion path of SM and EM of the metal for wiring; and thereby, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved. Further, by this aspect, the circuit delay can be improved; and a high performance metal for wiring can be provided.

[0147]

Also, according to the present invention recited above, a predetermined element, having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added to a metal for wiring having Cu as the main component; and therefore, the added element may be introduced in high concentration in the Cu crystal grain boundary and the crystal grain boundary proximity recited above. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved.

[0148]

Also, according to the present invention recited above, a stable intermetallic compound or a metal oxide is formed at the Cu crystal grain boundary and the crystal grain boundary proximity (outermost surface of the Cu crystal grain) which form the diffusion path for SM and EM; and thereby, the migration of Cu along the Cu crystal grain boundary can be inhibited; the oxidation of Cu in the metal for wiring is prevented; and the reliability of the metal for wiring can be improved.

[0149]

Also, according to the present invention recited above, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form the diffusion path for SM and EM; and on the other hand, a configuration is formed in which the crystal grain interior contains an ultra trace amount of added element of at most 0.1 atomic %; and thereby, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring is improved.

[0150]

According to the semiconductor device of the present invention, an added element is introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity which form the diffusion path for SM and EM of the metal wiring of the semiconductor device; and thereby, the migration of Cu along the Cu crystal grain boundary can be inhibited; and a semiconductor device can be provided having improved reliability of the metal wiring. Further, by this aspect, the circuit delay can be improved; and a semiconductor device can be provided having high performance metal wiring.

[0151]

According to the manufacturing method of the metal for wiring of the present invention, Cu crystal grains are grown in the Cu multicrystal formation step, and an added element is introduced into the Cu multicrystal; and therefore, inhibition of the grain growth of Cu due to the effects of an added element during heat treatment, such as that seen in the case where a Cu alloy seed layer is formed in a film using a sputter target having a mixture of several % of the added element, does not occur. Also, almost none of the added element exists in the bulk Cu; and therefore, electron scattering in the bulk Cu due to the added element can be inhibited; and the resistance of the Cu wiring can be reduced. As a result, the circuit delay can be improved; and a metal for wiring can be provided having high performance, excellent SM resistance and EM resistance, and high reliability.

[0152]

Also, according to the present invention recited above, the added element layer formation step and the added element diffusion step are performed simultaneously, thereby omitting steps and enabling easier manufacturing of the metal for wiring.

[0153]

Also, according to the present invention recited above, a predetermined element, having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added to a metal for wiring having Cu as the main component; and therefore, the added element can be introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal for wiring can be improved.

[0154]

According to the manufacturing method of the semiconductor device of the present invention, Cu crystal grains are grown in the Cu multicrystal formation step, and an added element is introduced into the Cu multicrystal; and therefore, inhibition of the Cu crystal grain growth due to the effects of an added element during heat treatment, such as that seen in the case where a Cu alloy seed layer is formed in a film using a sputter target having a mixture of several % of the added element, does not occur. Also, almost none of the added element exists in the bulk Cu; and therefore, electron scattering in the bulk Cu due to the added element can be inhibited; and the resistance of the Cu wiring of the semiconductor device can be reduced. As a result, the circuit delay can be improved; and a semiconductor device can be provided including a metal for wiring having high performance, excellent SM resistance and EM resistance, and high reliability.

[0155]

Also, according to the present invention recited above, the added element is introduced (diffused into the Cu) from the upper layer after the Cu is filled; and therefore, it becomes difficult for differences to occur in the concentrations of the added element due to different filling properties of Cu among the grooves and the holes

as seen in the case where a Cu alloy seed layer is formed in a film using a sputter target and the wiring grooves and the wiring holes are filled with Cu. As a result, variation of the resistivity of the Cu wiring according to the width of the wiring grooves is eliminated.

[0156]

Also, according to the present invention recited above, a barrier metal film is provided between the Cu and the insulative film; and therefore, diffusion of Cu into the insulative film and corrosion of the Cu can be prevented.

[0157]

Also, according to the present invention recited above, the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed prior to the excess Cu removal step; and thereby, a stable intermetallic compound can be formed between the Cu and the added element at the Cu crystal grain boundary and the crystal grain boundary proximity; and thereby, the EM resistance and SM resistance are improved; and the reliability of the metal wiring of the semiconductor device increases.

[0158]

Also, according to the present invention recited above, the added element layer formation step, the added element diffusion step, and the excess added element removal step are performed after the excess Cu removal step; and thereby, a stable intermetallic compound is formed between the Cu and the added element on the Cu crystal grain surface contacting the layer formed on the Cu which is the metal for wiring; the adhesion between Cu which is the metal for wiring and the upper layer improves; and the reliability of the metal wiring of the semiconductor device increases.

[0159]

According to the present invention recited above, the added element layer formation step and the added element diffusion step can be performed simultaneously, thereby omitting steps and enabling easier manufacturing of the semiconductor device.

[0160]

According to the present invention recited above, a predetermined element, having a solid solubility limit in Cu of at most 1 atomic % and a high diffusion coefficient at the Cu crystal grain boundary, is added into metal wiring of a semiconductor device having Cu as the main component; and therefore, the added element can be introduced in high concentration into the Cu crystal grain boundary and the crystal grain boundary proximity. Therefore, the migration of Cu along the Cu crystal grain boundary can be inhibited; and the reliability of the metal wiring of the semiconductor device can be improved.

[Brief Description of the Drawings]

[Fig. 1]

A cross-sectional view of a semiconductor device of a first exemplary embodiment of the present invention.

[Fig. 2]

A cross-sectional view describing a manufacturing method of the semiconductor device of the first exemplary embodiment of the present invention.

[Fig. 3]

A cross-sectional view of a semiconductor device of a second exemplary embodiment of the present invention.

[Fig. 4]

A cross-sectional view describing a manufacturing method of the semiconductor device of the second exemplary embodiment of the present invention.

[Fig. 5]

A cross-sectional view of a semiconductor device of a third exemplary embodiment of the present invention.

[Fig. 6]

A cross-sectional view describing a manufacturing method of the semiconductor device of the third exemplary embodiment of the present invention.

[Fig. 7]

A cross-sectional view describing front stage steps of a manufacturing method of a

semiconductor device of an example of the present invention.

[Fig. 8]

A cross-sectional view describing back stage steps of the manufacturing method of the semiconductor device of the example of the present invention.

[Fig. 9]

A cross-sectional view describing a manufacturing method of a semiconductor device of prior art.

[Fig. 10]

A cross-sectional view describing another example of a manufacturing method of a semiconductor device of prior art.

[Fig. 11]

A graph describing a relation between a storage time and a relative defect rate of via chains manufactured by the example and a comparison example.

[Fig. 12]

A graph illustrating the electromigration resistance of connection holes of via chains manufactured by the example and the comparison example by a relation between the cumulative time and the cumulative failure probability.

[Fig. 13]

A graph illustrating changes in resistivities of Cu wiring due to differences in heat treatments after Cu layer film formation of blanket film samples of the example.

[Fig. 14]

A graph illustrating distributions of Ti, Cu, and N of the barrier metal film, the Cu layer, and the added element layer of a blanket film sample of the example.

[Fig. 15]

A graph illustrating changes of resistivity of the Cu wiring due to differences in added elements and differences in heat treatment after the added element layer formation for blanket film samples of the example.

[Explanation of Reference Numerals]

1a, 1b, 1c, 1d: Insulative film

2a, 2b: Stopper insulative film

3a, 3b: Barrier metal film

4a, 4b: Cu layer

5a, 5b: Added element layer for adding to Cu

6a, 6b, 6c: Bulk Cu (crystal grain interior)

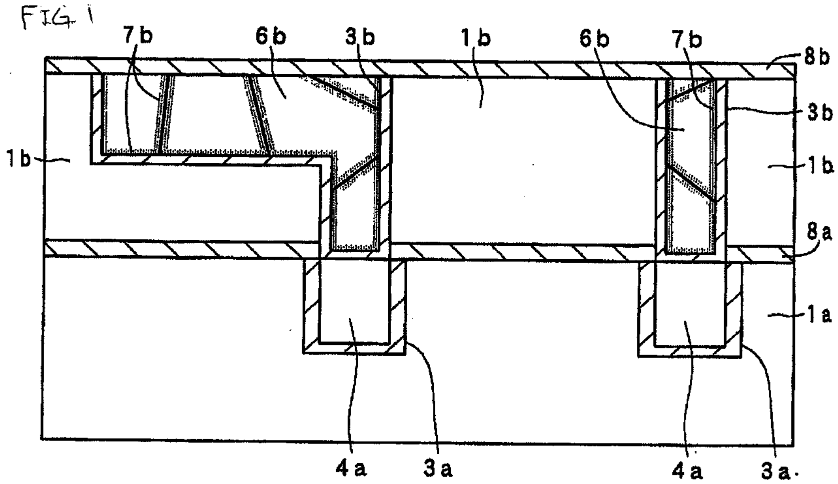
7a, 7b, 7c: Interface between Cu crystal grain boundary and a layer other than Cu

8a, 8b: Barrier insulative film

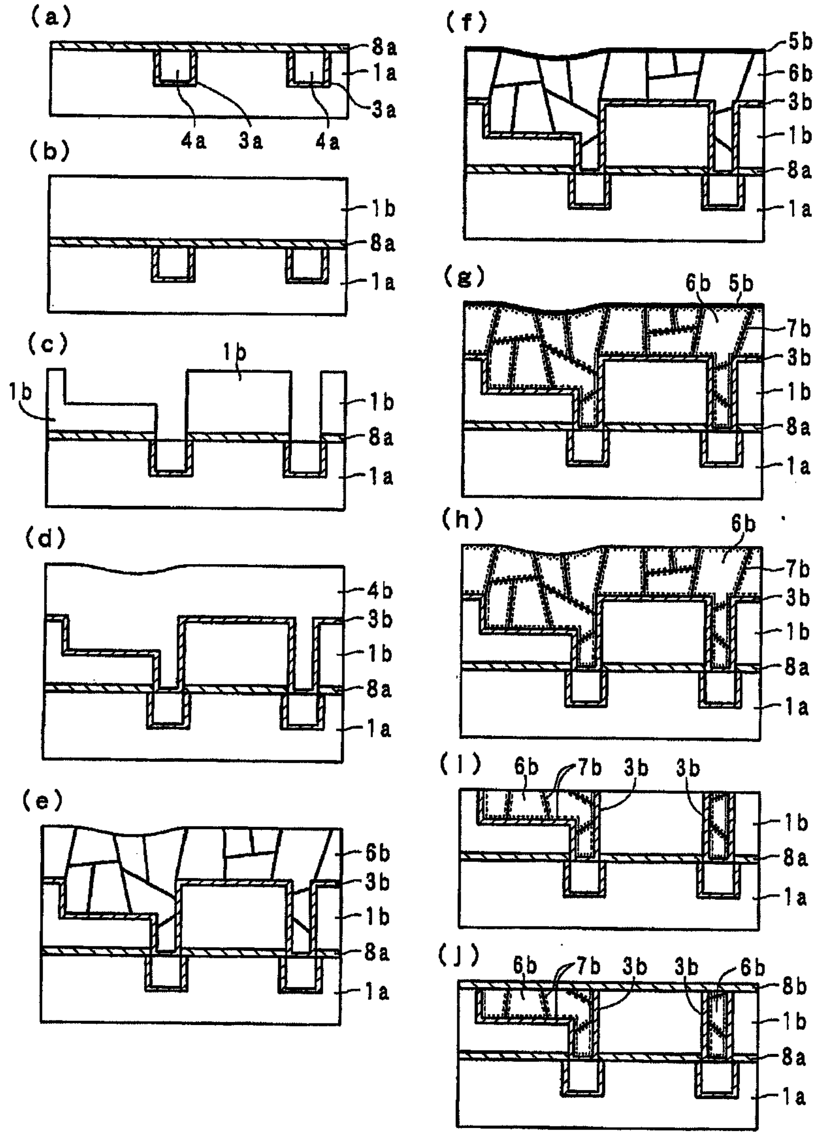
9: Cover insulative film

10b: Seed layer

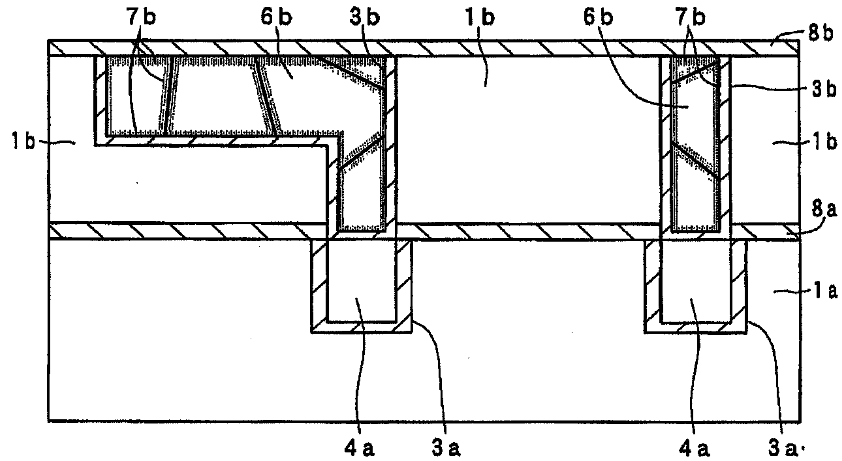
【書類名】　図面
[Name of Document]　Drawings
【図１】
FIG 1



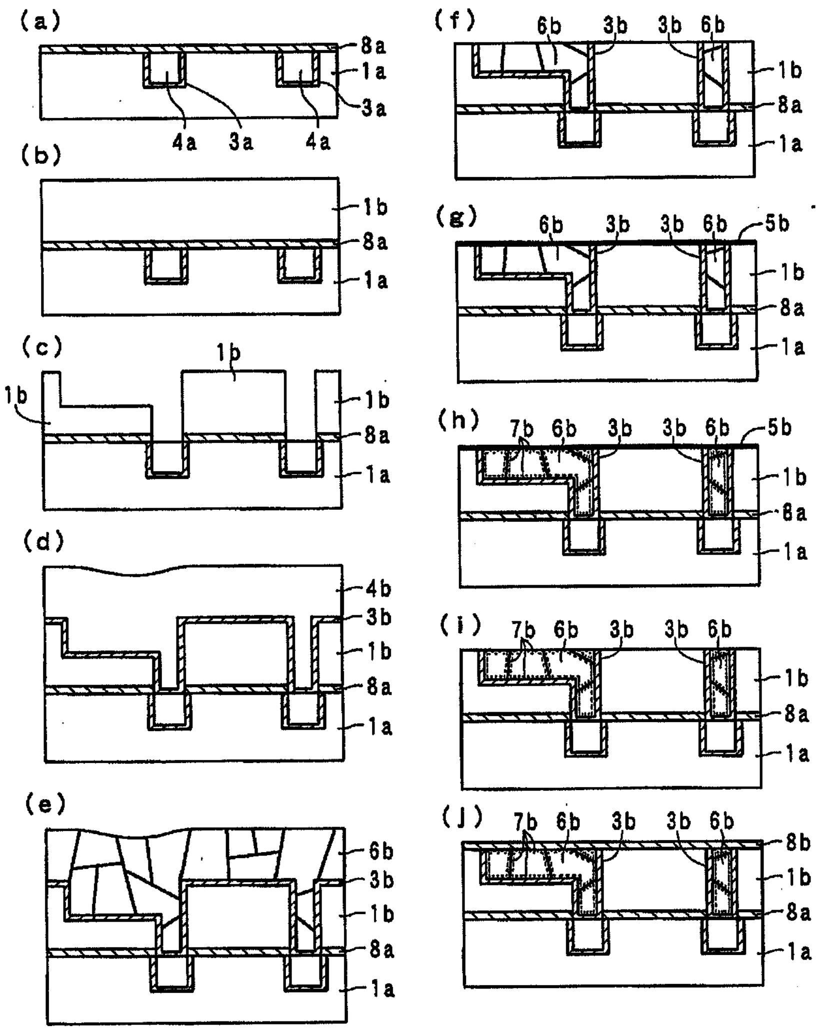
【図２】FIG.2


(a)
8a
1a
3a
4a
3a
4a
(b)
1b
8a
1a
(c)
1b
1b
1b
8a
1a
(d)
4b
3b
1b
8a
1a
(e)
6b
3b
1b
8a
1a
(f)
5b
6b
3b
1b
8a
1a.
(g)
6b
5b
7b
3b
1b
8a
1a
(h)
6b
7b
3b
1b
8a
1a
(I)
6b
7b
3b
3b
1b
8a
1a
(J)
6b
7b
3b
3b
6b
8b
1b
8a
1a

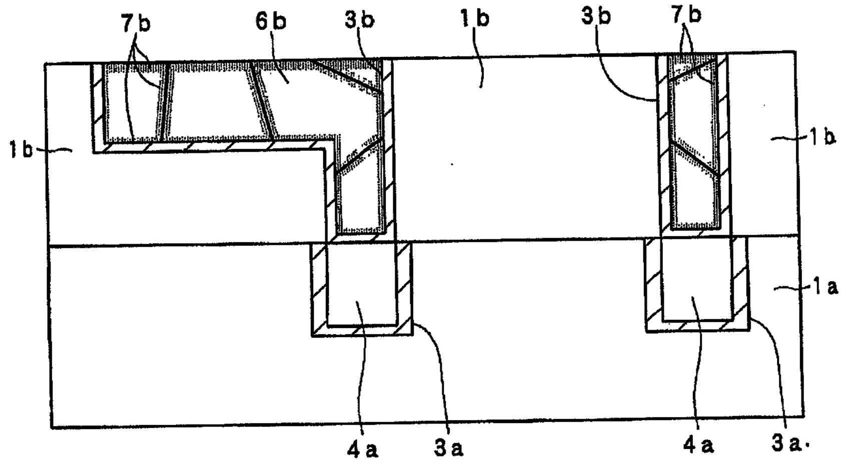
【図３】 FIG.3



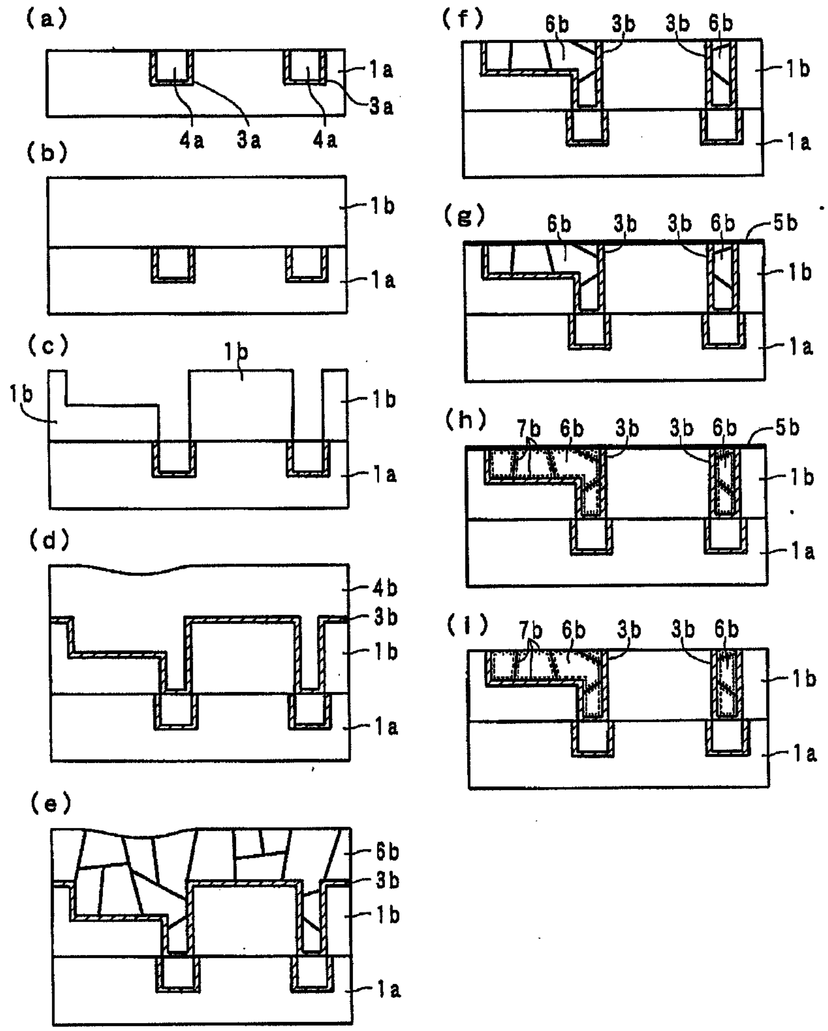
【図４】 FIG. 4


(a)
8a
1a
3a
4a
3a
4a
(b)
1b
8a
1a
(c)
1b
1b
1b
8a
1a
(d)
4b
3b
1b
8a
1a
(e)
6b
3b
1b
8a
1a
(f)
6b
3b
3b
6b
1b
8a
1a
(g)
6b
3b
3b
6b
5b
1b
8a
1a
(h)
7b
6b
3b
3b
6b
5b
1b
8a
1a
(i)
7b
6b
3b
3b
6b
1b
8a
1a
(J)
7b
6b
3b
3b
6b
8b
1b
8a
1a

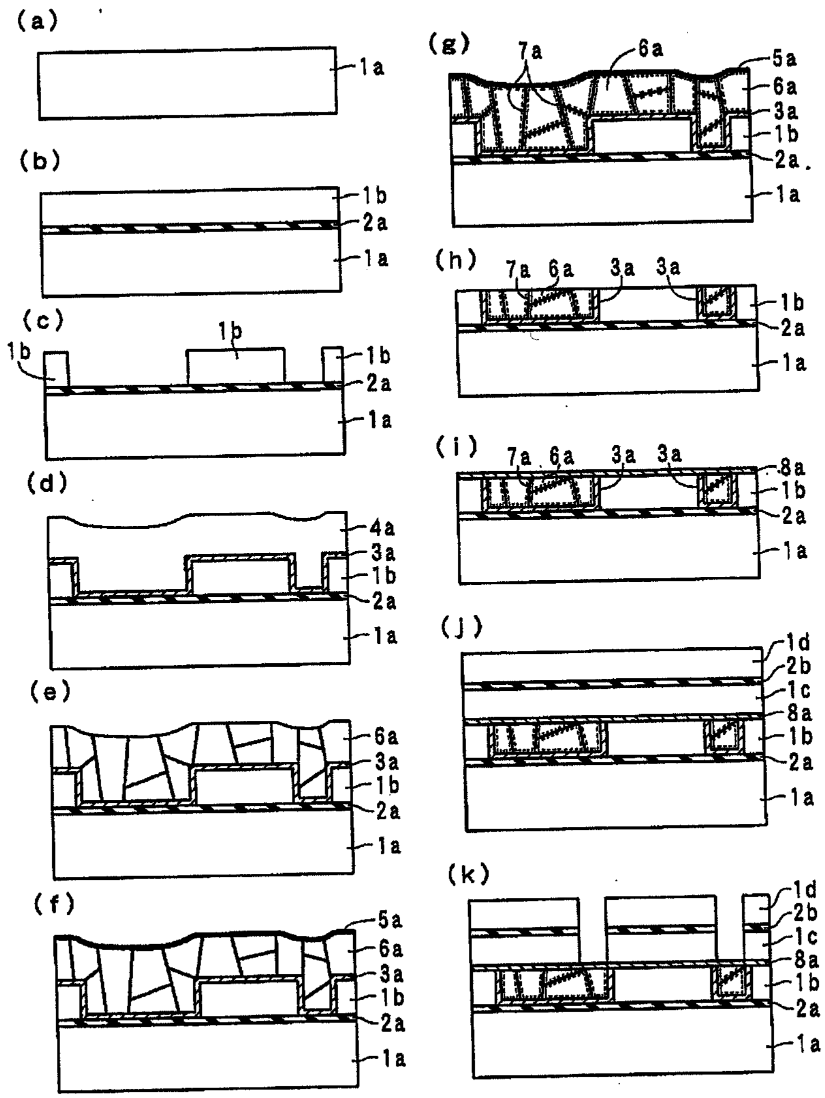
【図５】 FIG.5



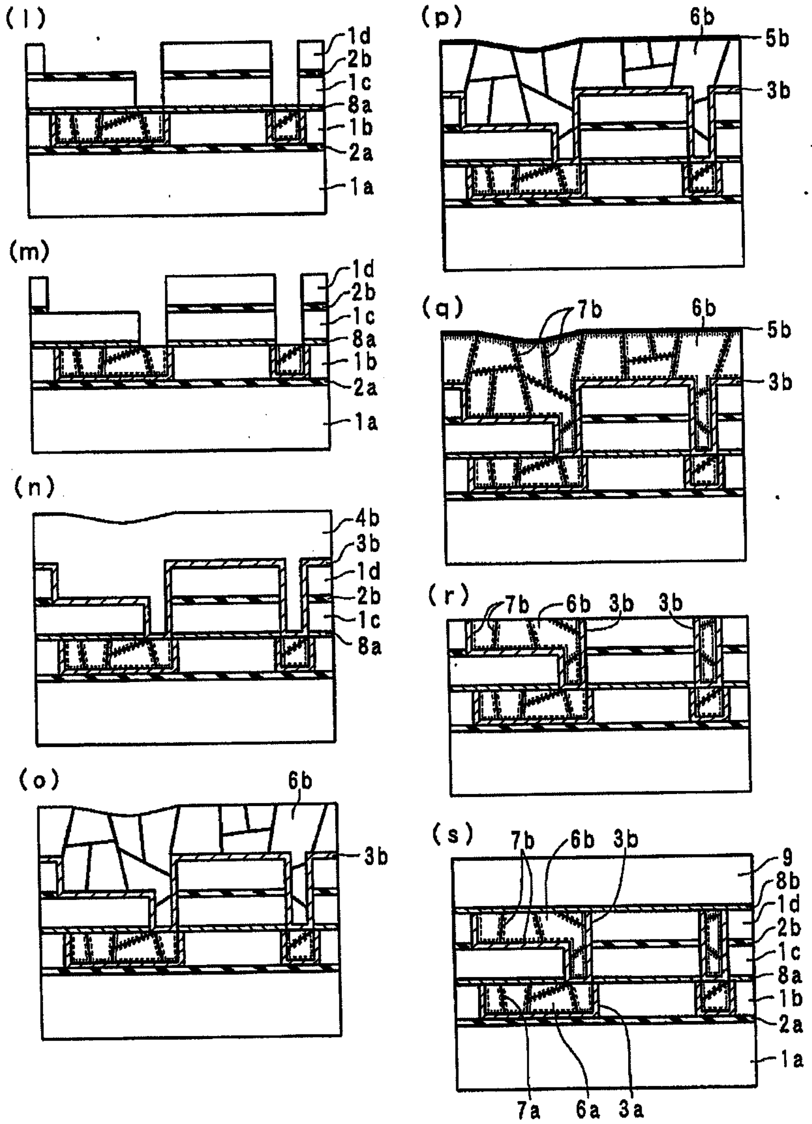
【図６】FIG. 6


(a)
1a
3a
4a
3a
4a
(b)
1b
1a
(c)
1b
1b
1b
1a
(d)
4b
3b
1b
1a
(e)
6b
3b
1b
1a
(f)
6b
3b
3b
6b
1b
1a
(g)
6b
3b
3b
6b
5b
1b
1a
(h)
7b
6b
3b
3b
6b
5b
1b
1a
(i)
7b
6b
3b
3b
6b
1b
1a

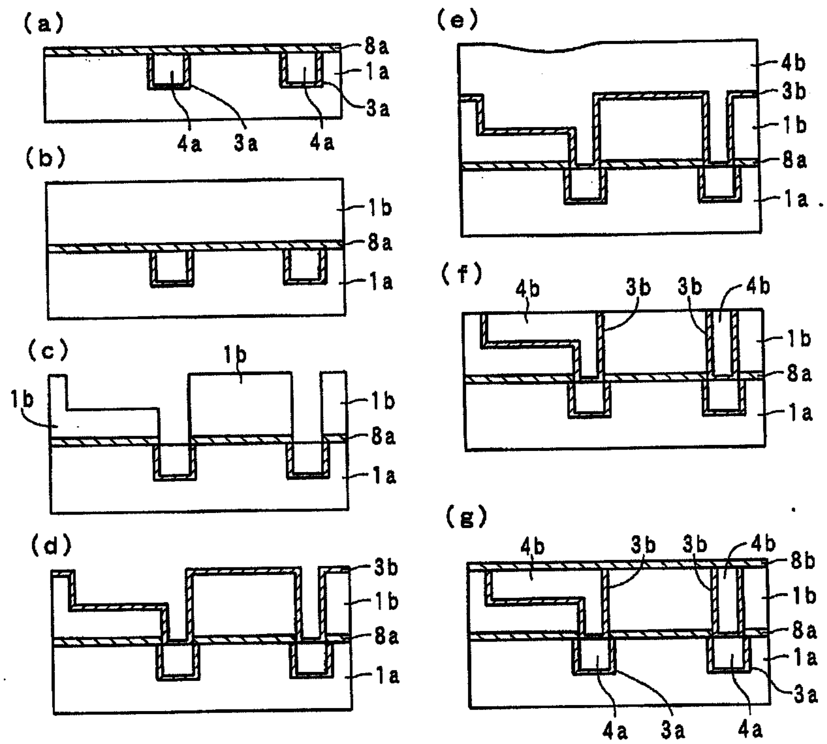
【図7】 FIG. 7


(a)
1a
(b)
1b
2a
1a
(c)
1b
1b
1b
2a
1a
(d)
4a
3a
1b
2a
1a
(e)
6a
3a
1b
2a
1a
(f)
5a
6a
3a
1b
2a
1a
(g)
7a
6a
5a
6a
3a
1b
2a
1a
(h)
7a
6a
3a
3a
1b
2a
1a
(i)
7a
6a
3a
3a
8a
1b
2a
1a
(j)
1d
2b
1c
8a
1b
2a
1a
(k)
1d
2b
1c
8a
1b
2a
1a

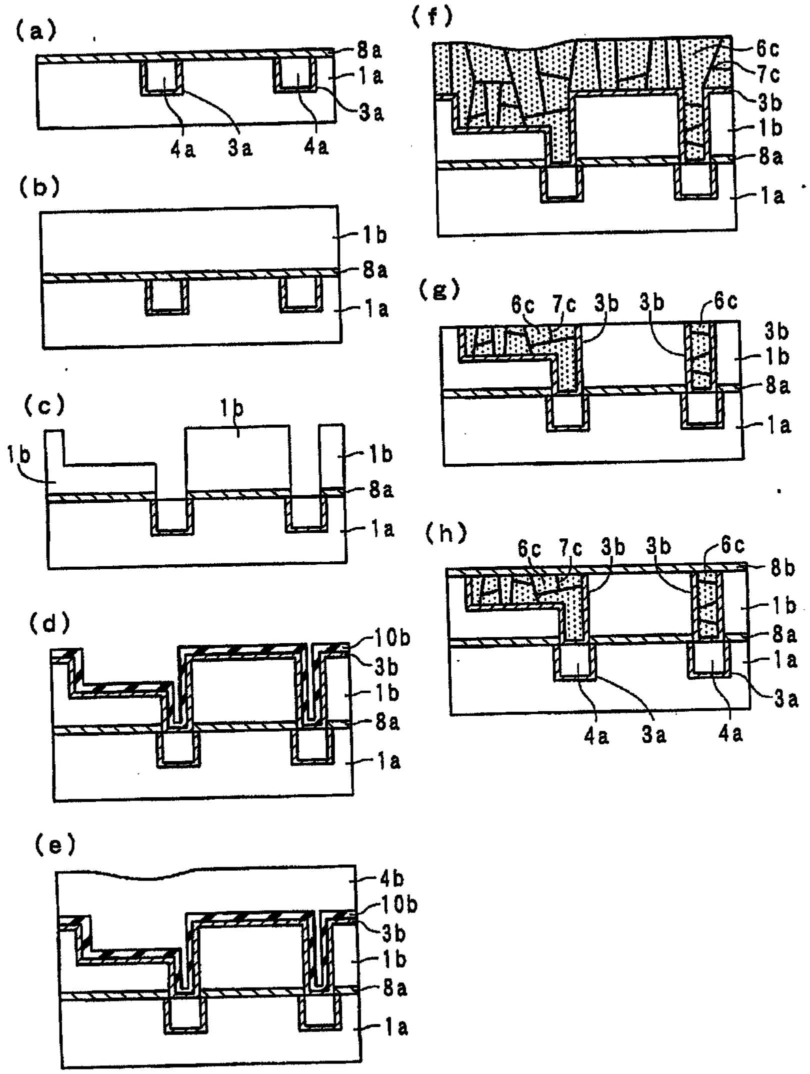
【図８】 FIG. 8


(l)
1d
2b
1c
8a
1b
2a
1a
(m)
1d
2b
1c
8a
1b
2a
1a
(n)
4b
3b
1d
2b
1c
8a
(o)
6b
3b
(p)
6b
5b
3b
(q)
7b
6b
5b
3b
(r)
7b
6b
3b
3b
(s)
7b
6b
3b
9
8b
1d
2b
1c
8a
1b
2a
1a
7a
6a
3a

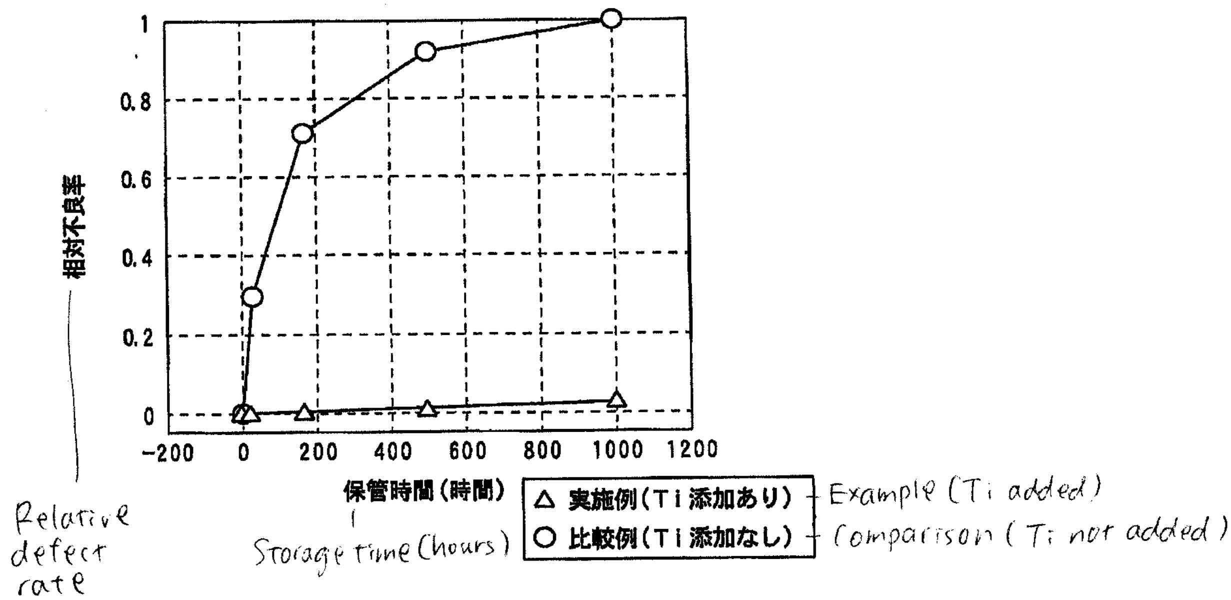
【図９】 FIG.9


(a)
8a
1a
3a
4a
3a
4a
(b)
1b
8a
1a
(c)
1b
1b
1b
8a
1a
(d)
3b
1b
8a
1a
(e)
4b
3b
1b
8a
1a
(f)
4b
3b
3b
4b
1b
8a
1a
(g)
4b
3b
3b
4b
8b
1b
8a
1a
3a
4a
3a
4a

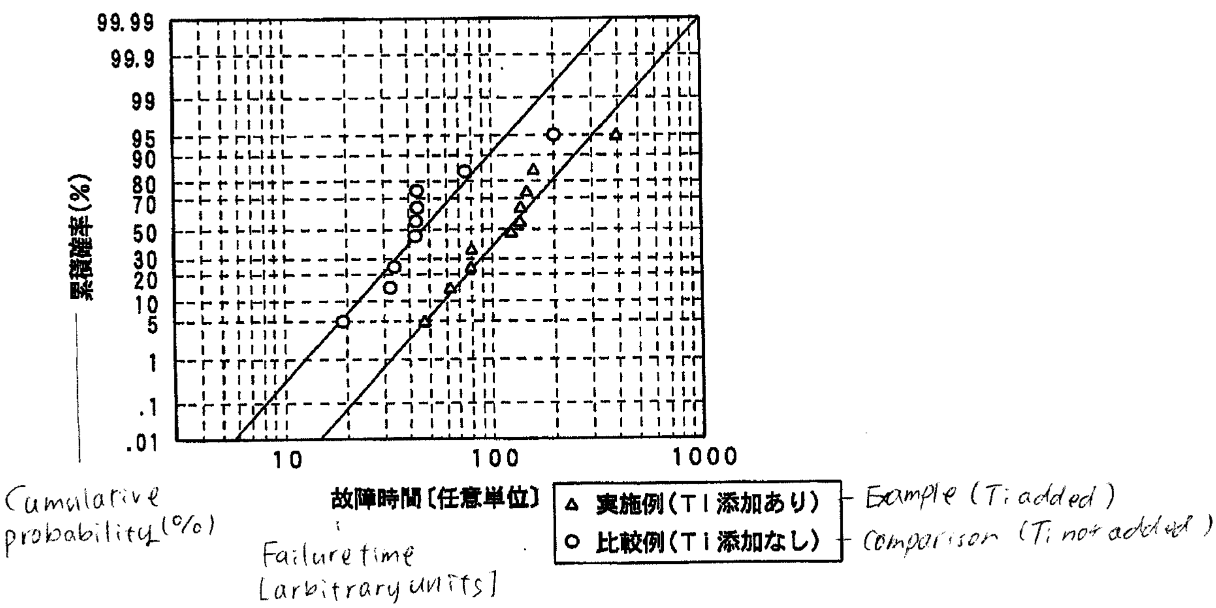
【図１０】 FIG.10


(a)
8a
1a
3a
4a
3a
4a
(b)
1b
8a
1a
(c)
1b
1b
1b
8a
1a
(d)
10b
3b
1b
8a
1a
(e)
4b
10b
3b
1b
8a
1a
(f)
6c
7c
3b
1b
8a
1a
(g)
6c
7c
3b
3b
6c
3b
1b
8a
1a
(h)
6c
7c
3b
3b
6c
8b
1b
8a
1a
3a
4a
3a
4a

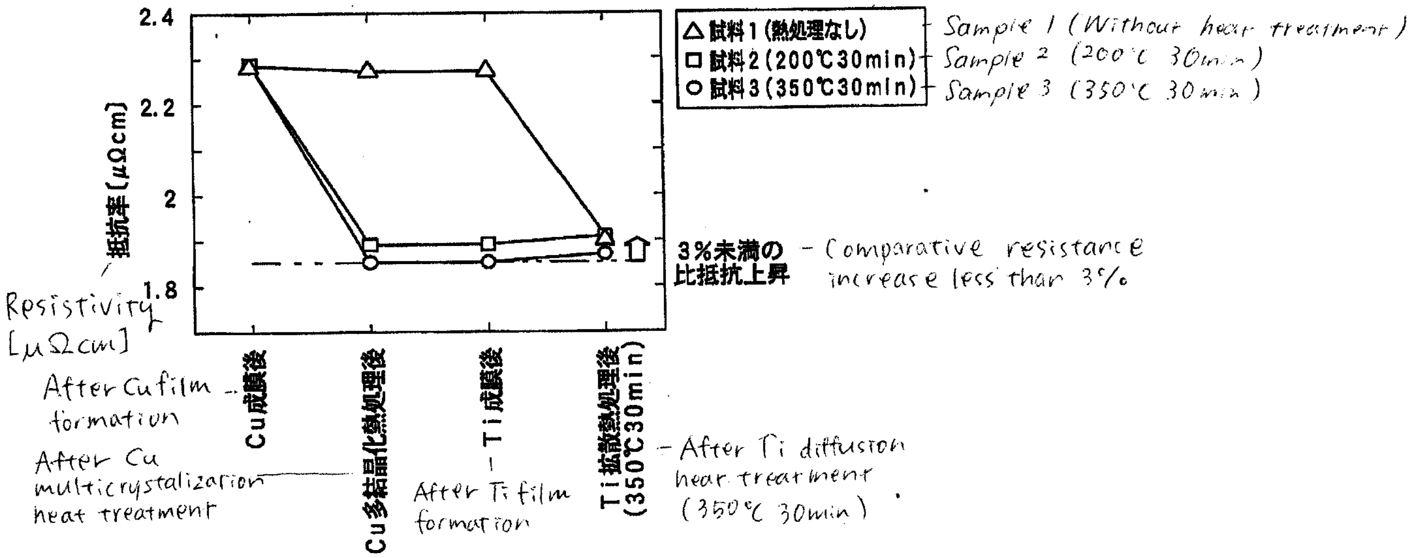
【図１１】 FIG. 11



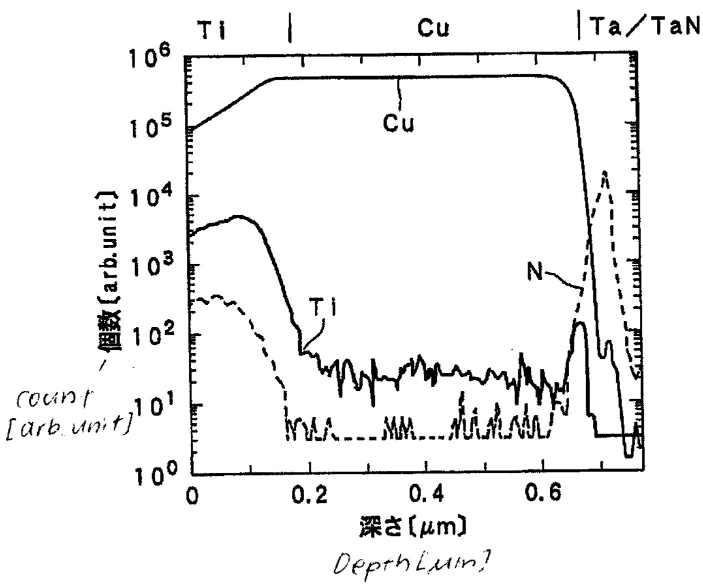
【図１２】 FIG. 12



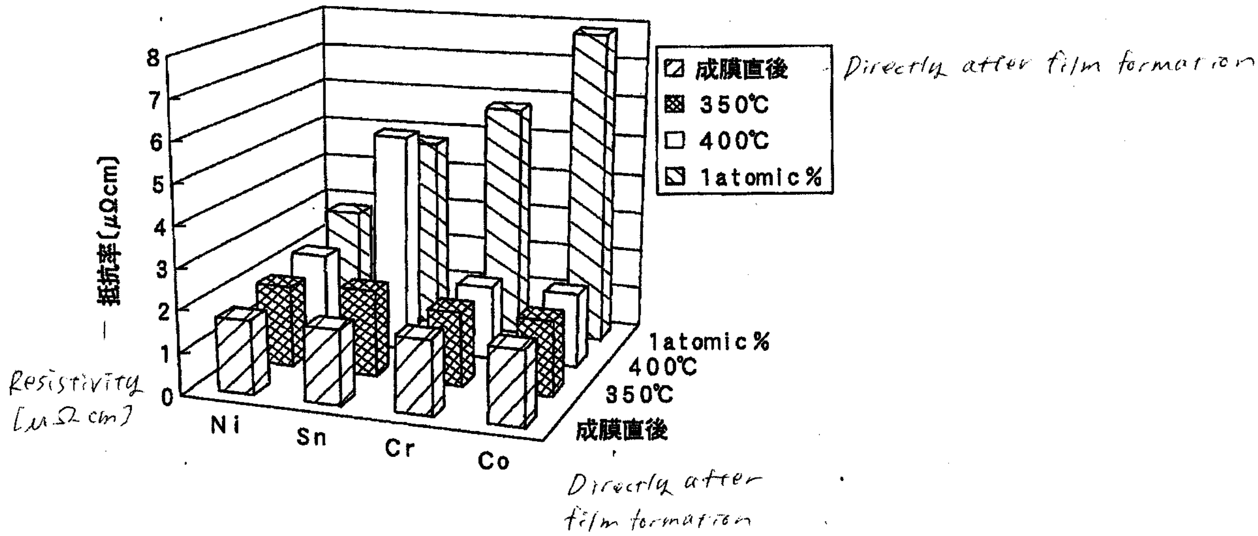
【図１３】 FIG.13



【図１４】 FIG.14



【図１５】 FIG. 15


8
7
6
5
4
3
2
1
0
抵抗率〔μΩcm〕
Resistivity [μΩ cm]
成膜直後
Directly after film formation
350℃
400℃
1atomic％
Ni
Sn
Cr
Co
1atomic％
400℃
350℃
成膜直後
Directly after film formation

[Name of Document] Abstract

[Abstract]

[Object] To improve circuit delay and provide: a metal for wiring having high performance, excellent SM (stress induced migration) resistance and EM (electromigration) resistance, and high reliability; a semiconductor device using the metal for wiring; and a manufacturing method therefor.

[Solution] A metal for wiring that contains a multicrystal having Cu (copper) as a main component and an added element other than Cu, characterized in that a concentration of the added element of a crystal grain boundary and a crystal grain boundary proximity of a crystal grain of the Cu multicrystal is larger than that of the crystal grain interior, solves the problems recited above. It is favorable that the added element is an element of at least any one of Ti, Zr, Hf, Cr, Co, Al, Sn, Ni, Mg, and Ag. The metal for wiring is manufactured by forming the Cu multicrystal, forming a layer of the added element on the Cu upper face, and diffusing the added element into the Cu. The metal for wiring may be used favorably as metal wiring formed in a semiconductor device.

[Selected Drawing] Fig. 1